ABSTRACT

A controller 102 and four flash memories F0 to F3 are connected by twos to two memory buses, and each flash memory is divided into two regions of substantially the same size to form a first half and a last half regions. In a four-memory configuration, a consecutive logical address specified by a host apparatus is divided into a predetermined size, and a write operation is performed in a format that repeatedly circulates through F0, F1, F2, F3 in this order. In a two-memory configuration, the write operation is performed in a format that repeatedly circulates through F00, F10, F01, F11. Thus, a controller processing is made common regardless of the number of flash memories connected to the controller.